Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

Claims 1-105 (canceled)

106. (currently amended) A semiconductor chip or wafer comprising:

a silicon substrate;

a ~~first~~ metallization structure over said silicon substrate~~, wherein said first metallization structure comprises a first contact pad~~;

a passivation layer over said ~~first~~ metallization structure, wherein an opening in said passivation layer exposes a ~~said~~ first contact pad of said metallization structure, and wherein said passivation layer comprises an inorganic material; and

a metal trace ~~second metallization structure~~ over part of said passivation layer and over said first contact pad, wherein said metal trace ~~second metallization structure~~ comprises a gold layer with a thickness of between 2 and 100 μm, wherein said metal trace ~~second metallization structure~~ comprises a second contact pad connected to said first contact pad, and wherein the positions of said first and second contact pads from a top view are different.

107. (previously presented) The semiconductor chip or wafer of claim 106, wherein said passivation layer comprises a topmost nitride layer of said semiconductor chip or wafer.

108. (previously presented) The semiconductor chip or wafer of claim 106, wherein said passivation layer comprises a topmost oxide layer of said semiconductor chip or wafer.

109. (previously presented) The semiconductor chip or wafer of claim 106, wherein said passivation layer comprises a topmost CVD-formed layer of said semiconductor chip or wafer.

110. (currently amended) The semiconductor chip or wafer of claim 106, wherein said metal trace ~~second metallization structure~~ further comprises a titanium-containing ~~metal~~ layer under said gold layer~~, wherein said metal layer comprises titanium tungsten~~.

Claim 111 (canceled)

112. (previously presented) The semiconductor chip or wafer of claim 106, wherein said second contact pad is used to be wirebonded thereto.

113. (currently amended) The semiconductor chip or wafer of claim 106 further comprising a wirebond over ~~on~~ said second contact pad.

114. (currently amended) The semiconductor chip or wafer of claim 106 further comprising a metal bump over ~~on~~ said second contact pad.

115. (currently amended) The semiconductor chip or wafer of claim 106 further comprising a solder bump over ~~on~~ said second contact pad.

116. (currently amended) The semiconductor chip or wafer of claim 106 further comprising a topmost polymer layer over said passivation layer, wherein said metal trace ~~gold layer~~ is over said topmost polymer layer.

Claims 117-118 (canceled)

119. (previously presented) The semiconductor chip or wafer of claim 106, wherein said gold layer is electroplated.

120. (currently amended) A semiconductor chip or wafer comprising:

a silicon substrate;

a ~~first~~ metallization structure over said silicon substrate~~, wherein said first metallization structure comprises a first contact pad~~;

a passivation layer over said ~~first~~ metallization structure, wherein an opening in said passivation layer exposes a ~~said~~ first contact pad of said metallization structure, and wherein said passivation layer comprises an inorganic material; and

a second contact pad connected to said first contact pad, wherein said second contact pad comprises a gold layer with a thickness of between 2 and 15 μm ~~100 μm~~ and is used to be wirebonded thereto.

Claims 121 and 122 (canceled)

123. (previously presented) The semiconductor chip or wafer of claim 120 further comprising a polymer layer over said passivation layer, wherein said second contact pad is over said polymer layer.

Claims 124 and 125 (canceled)

126. (previously presented) The semiconductor chip or wafer of claim 120, wherein said passivation layer comprises a topmost nitride layer of said semiconductor chip or wafer.

127. (previously presented) The semiconductor chip or wafer of claim 120, wherein said passivation layer comprises a topmost oxide layer of said semiconductor chip or wafer.

128. (previously presented) The semiconductor chip or wafer of claim 120, wherein said passivation layer comprises a topmost CVD-formed layer of said semiconductor chip or wafer.

129. (previously presented) The semiconductor chip or wafer of claim 120, wherein said gold layer is electroplated.

Claim 130 (canceled)

131. (currently amended) The semiconductor chip or wafer of claim 120 further comprising a wirebond over ~~on~~ said second contact pad.

Claims 132-135 (canceled)

136. (new) A circuitry component comprising:

a semiconductor substrate;

a metallization structure over said semiconductor substrate;

a passivation layer over said metallization structure, wherein said metallization structure comprises a first pad exposed by an opening in said passivation layer, and wherein said passivation layer comprises an inorganic material; and

a metal trace over said passivation layer, wherein said metal trace comprises a gold layer with a thickness of between 2 and 100 μm.

137. (new) The circuitry component of claim 136, wherein said metal trace comprises a pad used to be wirebonded thereto.

138. (new) The circuitry component of claim 136, wherein said metal trace comprises a pad used to have a metal bump formed thereon.

139. (new) The circuitry component of claim 136, wherein said metal trace comprises a titanium-containing layer under said gold layer.

140. (new) The circuitry component of claim 136, wherein said gold layer is electroplated.